Claims

1. A method for forming a capacitor device comprising the steps of:

forming a substrate;

forming a first interlayer dielectric layer on said substrate;

forming two or more contact plugs through said substrate, said plugs being separated from one another by a surface;

forming a conducting layer on said first interlayer dielectric layer;

producing an electrode on alternate ones of said two or more contact plugs by etching said conducting layer;

coating said electrodes with a ferroelectric layer;

etching said ferroelectric layer from said surfaces separating said contact plugs; and

creating additional electrodes by filling spaces between said electrodes on alternate ones of said contact plugs with a conductive material to establish electrical contact between the plugs and the electrodes.

2. A method according to claim 1, wherein the step of forming said first interlayer dielectric layer comprises forming said first interlayer dielectric layer of TEOS.

3. A method according to claim 1, wherein the step of forming said first interlayer dielectric layer comprises forming said first interlayer dielectric layer of silicon dioxide.

4. A method according to claim 1, wherein the step of forming a conducting layer on said first interlayer dielectric layer comprises forming said conducting layer of iridium.

5. A method according to claim 1, wherein the step of forming a conducting layer on said first interlayer dielectric layer comprises forming said conducting layer of iridium oxide.

6. A method according to claim 1, wherein the step of etching said ferroelectric layer from said surfaces separating said contact plugs comprises the step of applying a layer of hard mask material to said conducting layer, applying a photolithographic layer to said layer of hard mask material, exposing said photolithographic layer, and developing said exposed photolithographic layer to produce an etch pattern for said conducting layer and said hard mask layer.

7. A method according to claim 1, wherein the step of coating said electrodes with a ferroelectric layer comprises coating said electrodes with PZT.

8. A method according to claim 1, wherein the step of filling spaces between said electrodes on alternate ones of said contact plugs with a conductive material comprises filling said spaces with iridium.

9. A method according to claim 1, wherein the step of filling spaces between said electrodes on alternate ones of said contact plugs with a conductive material comprises filling said spaces with iridium oxide.

10. A method according to claim 1, further comprising forming a first barrier layer on said first interlayer dielectric layer.

11. A method according to claim 10, wherein the step of forming said first barrier layer comprises forming said barrier layer of a material substantially resistant to oxygen diffusion.

12. A method according to claim 10, wherein the step of forming said first barrier layer comprises forming said barrier layer of aluminium oxide.

13. A method according to claim 1, further comprising applying a chemical mechanical polishing process to exposed surfaces of said electrodes and said ferroelectric layer after the step of creating additional electrodes.

14. A method according to claim 13 comprising forming a second barrier layer extending over said device after the step of applying a chemical mechanical polishing process.

15. A method according to claim 14, wherein the step of forming said second barrier layer comprises forming said barrier layer of a material substantially resistant to oxygen diffusion.

16. A method according to claim 15, wherein the step of forming said second barrier layer comprises forming said barrier layer of aluminium oxide.

17. A method according to claim 1, wherein the step of producing an electrode on alternate ones of said two or more contact plugs by etching said conducting layer comprises etching said electrodes so that adjacent electrodes taper in opposite directions.

18. A method according to claim 17, wherein the step of etching said electrodes so that adjacent electrodes taper in opposite directions comprises etching the sides of adjacent electrodes to be substantially parallel.

19. A method according to claim 1, wherein the step of coating said electrodes with a ferroelectric layer comprises applying a layer of ferroelectric

material having substantially uniform thickness along the length of the side faces of the electrodes coated by the ferroelectric layer.

20. A method according to claim 1, wherein the step of coating said electrodes with a ferroelectric layer comprises applying a layer of ferroelectric material such that portions of said ferroelectric layer material deposited on opposite sides of the electrodes on which they are deposited slope in opposite directions.

21. A method according to claim 1, wherein the step of coating said electrodes with a ferroelectric layer comprises applying a layer of ferroelectric material such that alternate portions of said ferroelectric layer material deposited on adjacent electrodes slope in the same direction.

22. A method according to claim 22, wherein the step of coating said electrodes with a ferroelectric layer comprises applying a layer of ferroelectric material such that portions of said ferroelectric layer deposited on opposite sides of the electrodes on which they are deposited slope at an angle of tilt from the vertical of between approximately 0.1 to 10 degrees.

23. An FeRAM device formed according to the method of claim 1.

24. A device comprising:

a substrate;

a first interlayer dielectric layer formed on said substrate;

two or more contact plugs through said substrate, said plugs being separated from one another by a surface;

a conducting layer formed on said first interlayer dielectric layer;

an electrode formed on alternate ones of said two or more contact plugs by etching said conducting layer;

a ferroelectric layer coating said electrodes; and

a conductive filler material deposited in spaces between said electrodes on alternate ones of said contact plugs to create additional electrodes.

25. A device according to claim 24, wherein said first interlayer dielectric layer comprises TEOS.

26. A device according to claim 24, wherein said first interlayer dielectric layer comprises silicon dioxide.

27. A device according to claim 24, wherein said conducting layer comprises iridium.

28. A device according to claim 24, wherein said conducting layer comprises iridium oxide.

29. A device according to claim 24, further comprising a layer of hard mask material applied to said conducting layer, and a photolithographic layer applied to said layer of hard mask material, said photolithographic layer being exposed and developed to produce an etch pattern for said conducting layer and said hard mask layer.

30. A device according to claim 24, wherein said ferroelectric layer comprises PZT.

31. A device according to claim 24, wherein said conductive filler material comprises iridium.

32. A device according to claim 24, wherein said conductive filler material comprises iridium oxide.

33. A device according to claim 24, further comprising a first barrier layer formed on said first interlayer dielectric layer.

34. A device according to claim 33, wherein said first barrier layer comprises a material substantially resistant to oxygen diffusion.

35. A device according to claim 33, wherein said first barrier layer comprises aluminium oxide.

36. A device according to claim 24, further comprising a second barrier layer extending over said device.

37. A device according to claim 36, wherein said second barrier layer comprises a material substantially resistant to oxygen diffusion.

38. A device according to claim 36, wherein the said second barrier layer comprises aluminium oxide.

39. A device according to claim 24, wherein adjacent electrodes taper in opposite directions.

40. A device according to claim 24, wherein adjacent electrodes taper in opposite directions such that the sides of adjacent electrodes are substantially parallel.

41. A device according to claim 24, wherein said layer of ferroelectric material has a substantially uniform thickness along the length of the side faces of the electrodes coated by the ferroelectric layer.

42. A device according to claim 24, wherein portions of ferroelectric layer material deposited on opposite sides of the electrodes on which they are deposited slope in opposite directions.

43. A device according to claim 24, wherein alternate portions of said ferroelectric layer material deposited on adjacent electrodes slope in the same direction.

44. A device according to claim 24, wherein portions of said ferroelectric layer deposited on opposite sides of the electrodes on which they are deposited slope at an angle of tilt from the vertical of between approximately 0.1 to 10 degrees.

45. A ferroelectric capacitor device comprising the device of claim 24.

46. An FeRAM device comprising the device of claim 24.

47. A ferroelectric capacitor device formed according to the method of claim 1.